REMARKS

This paper is responsive to the Office Action mailed from the Patent and Trademark Office on May 21, 2004, which has a shortened statutory period set to expire August 21, 2004.

Claims

Claims 1-25 are pending in the above-identified application. Claims 1-25 stand rejected under 35 USC 103 for the reasons set forth below.

In the present paper, Claims 15 is amended for clarity. Claims 1-25 remain as filed. Reconsideration and withdrawal of the rejections directed to the pending claims is respectfully requested in view of the following remarks.

Claim 15 is amended to correct an obvious typographical error. No new matter is entered.

Rejections Over Tcherniaev in view of Bogliolo and Clarke

Claims 1-8, 10-20 and 22-25 stand rejected under 35 USC 103 as being unpatentable over Tcherniaev in view of Bogliolo and Clarke. This rejection is traversed for the reasons set forth below.

Claim 1 recites (in pertinent part):

> ...representing a plurality of identical components in a reduced form as a circuit having a single instance of the identical component with encoding for each input of the single instance to represent corresponding inputs to all of the plurality of identical components and decoding for each output port of the single instance to create output ports for the corresponding outputs associated with all of the plurality of identical components...

As set forth in Applicant's specification, the "encoding for each input" and "decoding for each output" involves identifying

sub-circuits or submodules that are instantiated n+1 times, and compressing the n+1 instances into a single instance whose input ports are mapped to encoded nets and whose output values are decoded back to actual nets. For example, Applicant's Fig. 1 (reproduced below for reference) graphically depicts a multiple instantiation of a submodule M (see page 10):

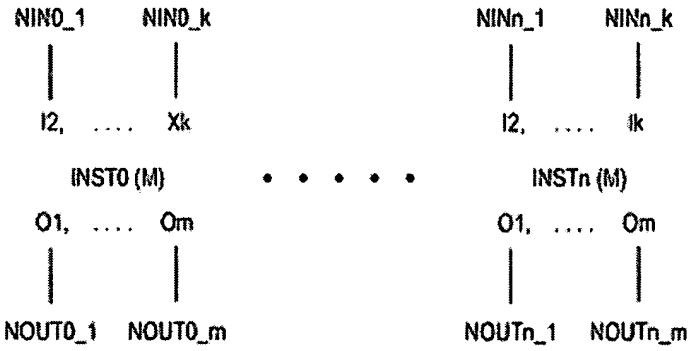

FIG. 1

Fig. 2 (also reproduced below) is a graphical depiction of a single instance whose input ports are mapped to the encoded nets of the separate instances, and whose output values are decoded back to actual nets (see pages 11-12):

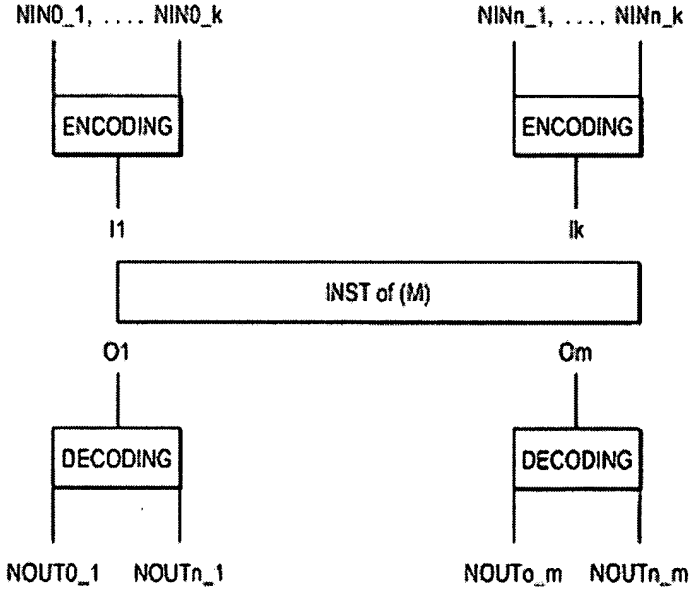

FIG. 2

Once the encoding and decoding have been created, the input encoding, the output decoding and the single instance of subcircuit M may be simulated. Symbolic simulation for the instance of M is performed and the non-compressed values for the output ports are obtained by the decoding process. Hence, as further recited in Claim 1:

> ...symbolically simulating the reduced form of the circuit with simulation results being the same as results of symbolically simulating the plurality of identical components.

Tcherniaev teaches a transistor level circuit simulator using a heirarchical representation of a circuit in which, once generated, the hierarchical representation may be used during simulation of the circuit to reduce the number of computations required (see abstract). In contrast to the method recited in Claim 1, however, Tcherniaev teaches (Col. 10, lines 10-17, reproduced below for reference) that the reduction in computations is achieved by eliminating the computations and storage for subcircuit instances with identical static subcircuit storage and dynamic state:

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According to the present invention, the reduction in computations as well as required memory may be achieved by eliminating the computations and storage for subcircuit instances with identical static subcircuit storage and dynamic state. As will be shown and described, during transient simulation, such duplicate storage and computations may be eliminated for subcircuit instances sharing static subcircuit storage and dynamic state.

Tcherniaev then provides an example in which two instances of a subcircuit having identical dynamic voltage states are identified, and duplicate storage and computation is eliminated by using a pointer to share the common dynamic voltage state (Col. 10, lines 10-17, and Fig. 2C, both reproduced below for reference:

In addition to sharing an equivalent circuit structure and therefore static subcircuit storage, two subcircuit instances may have an equivalent dynamic voltage state obtained during transient simulation. As shown in FIG. 2C, multiple instances **224**, **226**, **228** of the same subcircuit definition may share the same static subcircuit storage **212** as described above. In addition, the first instance **224** is shown to have a first dynamic voltage state **230** while the second instance **226** is shown to have a second dynamic voltage state **232**. The third instance **228** has a third dynamic voltage state **234** identical to that of the first dynamic voltage state **230**. In this case, there is no need to allocate a separate dynamic state for instance **228**. Rather, one or more pointers or other mechanisms may be used to permit both the first instance **224** and the third instance **228** to share this dynamic voltage state. As shown, the third instance **228** may provide a pointer from the third dynamic voltage state **234** to the first dynamic voltage state **230**. Alternatively, the dynamic voltage states may be represented as a set of voltage states associated with the specific subcircuit definition. Thus, each instance may provide its own pointer to the appropriate member of this set of dynamic voltage states.

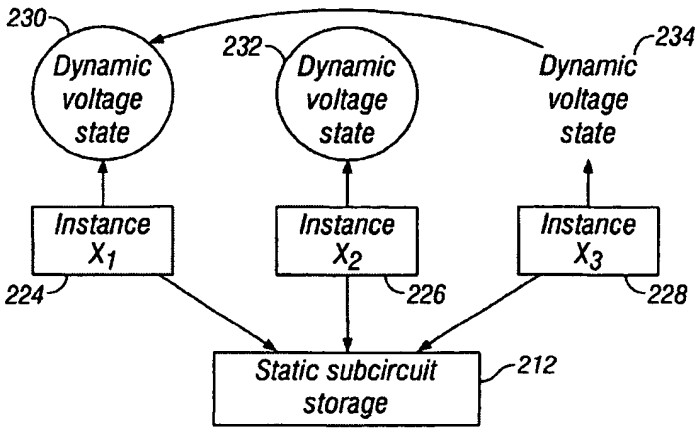


FIG. 2C

In rejecting Claim 1, the Examiner cites teachings from Columns 1-4 of Tcherniaev. Applicant respectfully points out that the generalized description cited by the Examiner is consistent with the detailed description reproduced above from Column 10 of Tcherniaev, and, at any rate, fails to either teach or suggest replacing the method quoted above with an encoding/decoding scheme.

Accordingly, it would not have been obvious to modify Tcherniaev to meet the limitations of Claim 1 at least because Tcherniaev fails to teach or suggest "representing a plurality of identical components in a reduced form as a circuit having a single instance of the identical component with encoding for each input of the single instance to represent corresponding inputs to all of the plurality of identical components and decoding for each output port of the single instance to create output ports for the corresponding outputs associated with all of the plurality of identical components", as recited in Claim 1.

Bogliolo and Clarke are cited for teaching symbolic simulation, and are not believed to overcome the deficiencies of Tcherniaev that are set forth above. Therefore, it would have been neither possible nor obvious to combine the teachings of Tcherniaev, Bogliolo and Clarke to produce the method recited in Claim 1.

Claims 2-8, 10 and 11 are dependent from Claim 1, and are distinguished over the cited prior arty for at least the reasons provided above with reference to Claim 1.

Claim 13 recites an apparatus including (in pertinent part) "means for representing a plurality of identical components in a reduced form as a circuit having a single instance of the identical component with encoding for each input of the single instance to represent corresponding inputs to all of the plurality of identical components and decoding for each output port of the single instance to create output ports for the outputs associated with all of the plurality of identical components". Therefore, Claim 13 is believed to be distinguished over Tcherniaev, Bogliolo and Clarke for reasons similar to those provided above with reference to Claim 1.

Claims 14-20 and 22-24 are dependent from Claim 13, and are distinguished over the cited prior arty for at least the reasons provided above with reference to Claim 13.

Claim 25 recites (in part) "an article of manufacture having one or more recordable media to store executable instructions which, when executed by a processing device, cause the processing device to: represent a plurality of identical components in a reduced form as a circuit having a single instance of the identical component with encoding for each input of the single instance to represent corresponding inputs to all of the plurality of identical components and decoding for each output port of the single instance to create output ports for

the outputs associated with all of the plurality of identical components". Therefore, Claim 25 is believed to be distinguished over Tcherniaev, Bogliolo and Clarke for reasons similar to those provided above with reference to Claim 1.

Rejections Over Tcherniaev, Bogliolo, Clarke, and Sangiovanni

Claims 9 and 21 stand rejected under 35 USC 103 as being unpatentable over Tcherniaev in view of Bogliolo, Clarke and Sangiovanni.

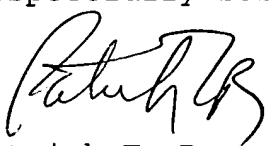
Claim 9 is dependent from Claim 1, and Claim 21 is dependent from Claim 13, both of which are distinguished over Tcherniaev in view of Bogliolo and Clarke for the reasons set forth above. Sangiovanni fails to overcome the deficiencies of these three references. Therefore, it would not have been possible to combine the teachings of Tcherniaev, Bogliolo, Clarke, and Sangiovanni to produce the method recited in Claims 1 and 13. Accordingly, Claims 9 and 21 are distinguished over these references for at least the reasons associated with Claims 1 and 13.

For the above reasons, Applicant respectfully requests reconsideration and withdrawal of the rejections under 35 USC 103.

CONCLUSION

Claims 1-25 are pending in the present application. Reconsideration and allowance Claims 1-25 is respectfully requested.

Respectfully submitted,



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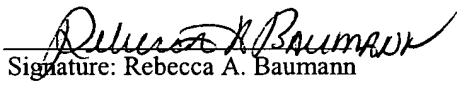
Signature: Rebecca A. Baumann